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Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Axel THOMSEN, Jerome E. JOHNSTON, Edwin DE ANGEL, Aryesh AMAR
FOR: AN INTEGRATED CIRCUIT WITH A MODE CONTROL SELECTING SETTLED AND UNSETTLED OUTPUT FROM A FILTER

Enclosed are:

- ☒ 18 pages of cover sheet, specification, claims, abstract.
- ☐ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☐ Certified copy of _____
- ☒ 29 sheets of formal drawing.
- ☐ An assignment of the invention to _____ and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ Information Disclosure Statement, Form PTO-1449 and reference.
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Respectfully submitted,

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Docket No: **50246-171**

APPLICATION FOR UNITED STATES LETTERS PATENT FOR

AN INTEGRATED CIRCUIT WITH A MODE CONTROL SELECTING SETTLED AND UNSETTLED OUTPUT FROM A FILTER

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Docket No. 50246-171

AN INTEGRATED CIRCUIT WITH A MODE CONTROL SELECTING SETTLED AND UNSETTLED OUTPUT FROM A FILTER

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority to U.S. Provisional Patent Application Serial No. 60/216,346, filed July 5, 2000, by inventors Axel Thomsen, Sherry Wu, Edwin de Angel, Aryesh Amar, Lei Wang, Eric J. Swanson and Jerome E. Johnston, entitled "ARNOLD PROVISIONAL" (Docket No. 50246-072) which is hereby incorporated by reference in its entirety.

This application is related to U.S. Patent Application Serial Number 09/054,542, filed April 3, 1998, by inventors Wai Laing Lee, Axel Thomsen and Dan Kasha, entitled "ANALOG TO DIGITAL SWITCHED CAPACITOR CONVERTER USING A DELTA-SIGMA MODULATOR HAVING VERY LOW POWER, DISTORTION AND NOISE" (Docket No. 0839-CS/50246-024).

This application is related to U.S. Patent Application Serial No. 09/321,583, filed May 28, 1999, by inventors Aryesh Amar, Jerome E. Johnston and Donald Keith Coffey, entitled "USE OF POINTERS TO ENHANCE FLEXIBILITY OF SERIAL PORT INTERFACE FOR AN INTEGRATED CIRCUIT WITH PROGRAMMABLE COMPONENTS" (Docket No. 0937-CS/50245-101).

This application is related to U.S. Patent Application Serial No. _____, filed October 25, 2000, by inventors Axel Thomsen and Lei Wang, entitled "TECHNIQUES FOR IMPLEMENTING A ROUGH BUFFER FOR CHARGING A SAMPLING CAPACITOR" (Docket No. 50246-071).

This application is related to U.S. Patent Application Serial No. _____, filed October 25, 2000, by inventors Axel Thomsen, Edwin de Angel, Sherry Wu, Lei Wang and Aryesh Amar, entitled "TECHNIQUES FOR SIGNAL MEASUREMENT USING A CONDITIONALLY STABLE AMPLIFIER" (Docket No. 50246-070).

This application is related to U.S. Patent Application Serial No. _____, filed

October 25, 2000, by inventor Edwin de Angel, entitled "A MULTIPLIER WITH EFFICIENT CARRY RIPPLE " (Docket No. 50246-073).

This application is related to U.S. Patent Application Serial No. _____, filed October 25, 2000, by inventors Aryesh Amar, Edwin de Angel and Eric J. Swanson, entitled "INDEPENDENT CONTROL OF CALIBRATION REGISTERS IN A MULTI CHANNEL A-D CONVERTER" (Docket No. 50246-074).

This application is related to U.S. Patent Application Serial No. _____, filed October 25, 2000, by inventor Axel Thomsen, entitled "INDIRECT TECHNIQUES FOR MEASURING 1/f NOISE" (Docket No. 50246-076).

This application is related to U.S. Patent Application Serial No. _____, filed October 25, 2000, by inventors Axel Thomsen, Edwin de Angel, Sherry Wu, Aryesh Amar and Jerome E. Johnston, entitled "APPLICATIONS OF A CONDITIONALLY STABLE INSTRUMENTATION AMPLIFIER TO INDUSTRIAL MEASUREMENT" (Docket No. 50246-077).

DOCKET #50246-077

FIELD OF THE INVENTION

The invention relates to signal measurement, and more particularly to signal measurement using a conditionally stable amplifier.

BACKGROUND OF THE INVENTION

Techniques for amplification of an analog signal, sampling and converting the signal to digital and processing that signal using digital techniques are known in the art.

Instrumentation amplifiers are commonly used to amplify values of an analog signal. Noise, distortion and offset are critical performance parameters.

Following an instrumentation amplifier in a signal processing chain is typically an analog to digital converter. At its input, the signal is sampled onto a capacitor. To reduce loading effects of the sample process used to sample an analog signal, a rough buffer may be used to precharge the sampling capacitor followed by a period of fine adjustment. The sampled analog signal is converted to digital, such as a one bit digital stream and filtered to produce a multibit digital signal.

Filters for doing such processing, such as FIR filters and FIR sinc filters are known. Some such filters may use coefficients for multiplying digital values. Others, such as

Hogenauer filters, described in an article by Eugene B. Hogenauer, entitled "AN ECONOMICAL CLASS OF DIGITAL FILTERS FOR DECIMATION AND INTERPOLATION," published in IEEE Transactions on Acoustics, Speech and Signal Processing, Volume ASSP-29, No. 2, April 1981, perform the filtering without coefficients.

A typical data acquisition system may consist of an ADC preceded by signal conditioning circuitry and followed by digital signal processing and communication circuits. Often the digital signal processing circuitry includes an FIR filter, typically performing the function of decimation and low pass filtering of the signal.

Any FIR filter will have a settling time. The function of the FIR can be described as

$$Y(z) = \mathrm{Sum}(A_i * X * z^{-1}$$

where A_i are the coefficients of the filter, X is the input, Y the output and i the index of the taps running from 1 to n. $X * z^{-1}$ then represents data delayed by i clock cycles.

SUMMARY OF THE INVENTION

When starting a conversion after a reset or a change of input channel, the filter will have an incomplete set of input data as the delayed inputs are all zero from the reset operation. During the time that data are filling up the pipeline of delayed data (until the nth sample of X), the calculation of Y will give a result that holds information about the input, but does not present the data with the same scaling and frequency content as the fully settled filter. Knowledge about the filter coefficients is required to extract information about the input from the unsettled data.

To some users these unsettled data may be useful information, to others they are not. If one were to provide unsettled data to a user who is only interested in settled data, there would be additional software overhead necessary to separate good from bad data.

The invention provides for a select bit that allows the user to specify whether or not he wants to see the unsettled data or only settled data. Any overhead of distinguishing between settled and unsettled data is pulled into the hardware implementation and thus requires no software overhead for the user.

The foregoing and other features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1.1A is a block diagram of an integrated circuit chip in accordance with one aspect of the invention.

Figure 1.1B is a block diagram of an integrated circuit chip having a mode select pin by which a user can specify settled or unsettled data in accordance with one aspect of the invention.

Figure 1.2A illustrates the integrated circuit of Figure 1.1A with more detail in the analog circuitry portion.

Figure 1.2B illustrates the integrated circuit of Figure 1.1A modified to inhibit output until a filter fully settles.

Figure 1.2C shows a typical FIR filter which can be used in accordance with the invention.

Figure 1.3 is a schematic diagram of an amplifier architecture used in conjunction with Figures 1.1 and 1.2, which includes chopper stabilization.

Figure 1.4 is a schematic diagram of an architecture of a delta sigma modulator in accordance with one aspect of the invention.

Figure 1.5A is a high level view of the digital portion of the chip illustrated in Figure 1.1.

Figure 1.5B is a view of Figure 1.5A, modified to include settled mode selection.

Figure 1.6A is a diagram showing an architecture of the serial port including serial interface and calibration and memory control logic.

Figure 1.6B is a diagram showing a modification of the serial port of Figure 1.6A to include settled mode selection.

Figure 2.0 is a high level schematic diagram of a rough buffer utilized in conjunction with amplifier 110 of figure 1.1.

Figure 2.1 is an implementation of a rough buffer with an n-type output stage.

Figures 2.2 and 2.3 show the step response of the rough buffer of Figure 2.1 to a negative step and to a positive step, respectfully.

Figure 2.4 shows implementation of a rough buffer with p-type output stage showing the slow and fast responses.

Figure 2.5 is a schematic diagram of an implementation of a complete rough buffer scheme including a comparator for selection of the proper output stage.

Figures 2.6, 2.7, and 2.8 show respectively an input voltage to the rough buffer, a comparator output from the rough buffer implementation shown in Figure 2.5 and the rough buffer output showing a fast response independent of input polarity.

Figure 3.1 is a block diagram of a multiplier architecture in accordance with the invention.

Figure 3.2 illustrates an encoding scheme utilized in conjunction with the multiplier architecture of Figure 3.1.

Figure 3.3 illustrates an expansion of the algorithm to show the carry propagate and coding scheme utilized with a multiplier architecture of Figure 1.

Figure 3.4 shows an example of the encoding scheme of Figures 3.2 and 3.3 as applied in the prior art.

Figure 3.5 illustrates a multiplication example using two's compliments in the encoding scheme of Figures 3.2.

Figure 4.1 is a register diagram of the serial port 140 showing calibration and SRAM/control logic 150 of Figure 1.1.

Figure 4.2 has an illustration of the serial port command structure.

Figure 4.3 shows more of the serial port command structure shown on Figure 4.2.

Figure 4.4 illustrates an example of how a command would be interpreted with dedicated physical channel, gain and offset relationships.

Figure 4.5 shows an example of pointers used to select a calibration register.

Figure 4.6 shows the new pointer based register allocation in accordance with one aspect of the invention.

Figure 5.1 shows a flow diagram of a test algorithm in accordance with one aspect of the invention.

Figures 6.1 shows a partial schematic, partial blocked diagram of the integrated circuit of Figure 1 used to measure the output of a thermal couple.

Figure 6.2 is a partial schematic, partial blocked diagram of the integrated circuit of Figure 1 used to measure the output of a bridge transducer.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1.1A is a block diagram of an integrated circuit chip in accordance with one aspect of the invention. At the left of Figure 1.1A, a number of analog input terminal pairs,

ain_i+ ain_i-, are shown. The number of analog input terminals is a matter of design choice. In some versions of the chip, only two input pairs are used, whereas in other implementations, four input pairs or more may be utilized. Each of the input pairs is fed to multiplexer 100 which selects the particular input to be applied to programmable instrumentation amplifier 110, described more hereinafter. The output of the programmable instrumentation amplifier 110 is applied to a differential fourth order ΔΣ modulator 120. Once the analog signal is converted to a digital bit stream, it is applied to programmable sinc FIR filter 130 where it is processed and ultimately converted to an output value to be sent to externally connected equipment over serial interface 140. Serial interface 140 contains or has associated with it calibration information storage and control logic 150. A clock generator 160 is used to generate internal timing on the chip.

A latched output 170 is utilized to control external logic. The input of 120 is analog and so everything before and up to the output of the differential fourth order ΔΣ modulator constitutes the analog portion of the signal processing. A separate analog power supply VA+ and VA- is available for this portion of the circuitry. In addition, a separate power source VD+ and DGND are available for powering the digital portion of the chip (e.g. items 130, 140, 150 and 160). A reference input V_{ref+} and V_{ref-} is used for the differential fourth order ΔΣ modulator. An externally supplied capacitor may be applied across terminal C1 and C2 of the programmable instrumentation amplifier 110 to implement antialias filtering.

Figure 1.1B is a block diagram of an integrated circuit chip having a mode select pin, labeled "mode" by which a user can specify settled or unsettled data in accordance with one aspect of the invention.

Figure 1.2A is a block diagram showing portions of the chip shown in Figure 1.1 in more detail. In this rendition, the multiplexer 100 shows two alternative configurations. The upper configuration shows a two input multiplexer whereas the bottom configuration shows a four input multiplexer. As discussed above, the number of signal pairs multiplexed is a matter of design choice.

Figure 1.2B illustrates the integrated circuit of Figure 1.1A modified to inhibit output until a filter, labeled "FIR Filter" fully settles.

Figure 1.2C shows a typical FIR filter which can be used in accordance with the invention. When starting a conversion after a reset or a change of input channel, the filter will have an incomplete set of input data as the delayed inputs are all zero from the

reset operation. During the time that data are filling up the pipeline of delayed data (until the nth sample of X), the calculation of Y will give a result that holds information about the input, but does not present the data with the same scaling and frequency content as the fully settled filter. However, if one has knowledge about the filter coefficients one may extract information about the input from the unsettled data; that is, knowing the number of delay increments from the time the input channel is reset or from the time when a new input channel is selected, together with the filter coefficients A_i, one may calculate the state of the input. Some user processes may have or may be modified to have such calculation capabilities.

Returning to Figure 1.2B, when a user requires fully settled information, the user selects settle mode by either applying a select voltage to the "mode" input pin of Figure 1.1B or by setting a settled mode bit as shown in Figure 1.6B hereafter.

Figure 1.3 is a diagram of a four stage chopper stabilized instrumentation amplifier using feed forward compensation utilized as the active amplification element for the programmable gain instrumentation amplifier shown in Figure 1.2. This amplifier is conditionally stable and uses multipath feed forward compensation and uses a plurality of integration stages I1 through I4. The characteristics of this type of amplifier are described in an article entitled "A FIVE STAGE CHOPPER STABILIZED INSTRUMENTATION AMPLIFIER USING FEED FORWARD COMPENSATION" by Axel Thomsen et al., presented at the VLSI Circuit Symposium 98, a copy of which is attached to the specification and which article is incorporated herein by reference in its entirety, and in U.S. Patent 6,002,299 by Axel Thomsen, which patent is also incorporated herein by reference in its entirety.

The multipath feedforward compensated amplifier is best suited for the low level signal measurement because of the following attributes. It allows for a implementation of chopper stalibization without noise penalties or large chopper artifacts. It also allows one to build a low distortion amplifier without large power consumption.

In a multipath amplifier with chopper stabilization, the offset is often dominated by the input referred offset of the second stage.

In the Multipath Architecture, the first integrator is often followed by attenuation to achieve low unity gain frequency of the integrator while maintaining low noise and reasonable device sizes.

An attenuator will act as gain when calculating the input referred offset of the amplifier. The addition of integrator I0 at the output of I1 before the attenuation reduces the second stage contribution by the attenuation factor used (in the Example 128x). Before V_{os} $=V_{os2} \cdot 128 \frac{1}{A_{v1}}$. After $V_{os} =V_{os2} \cdot 128 \cdot \frac{1}{A_{v1} A_{v0}} + V_{os1} \cdot \frac{1}{A_v}$

Figure 1.4 is a block diagram of a differential fourth ordered ΔΣ modulator shown in Figures 1.1 and 1.2. This ΔΣ modulator is described in U.S. Patent Application Serial No. 09/054,542, filed April 3, 1998, by inventors Wai Laing Lee, Axel Thomsen and Dan Kasha, and entitled ANALOG TO DIGITAL SWITCHED CAPACITOR CONVERTER USING A DELTA-SIGMA MODULATOR HAVING VERY LOW POWER, DISTORTION AND NOISE" (Docket No. 0839-CS/50246-024), referred to above, which application is incorporated herein in its entirety by reference. This type of ADC is very suitable for DC measurement applications. Other analog to digital conversion techniques can be applied here as well. It should be pointed out that it is easy to implement the delta sigma ADC in switched capacitor techniques and achieve a rail to rail input range.

As shown in Figure 1.1, the output of the differential fourth ordered ΔΣ modulator is applied to programmable sinc FIR filter 130.

Figure 1.5A shows an overview of the digital circuitry in more detail. Specifically shown is the two stage filter. It is a fixed rate $sinc^5$ followed by a selectable rate $sinc^3$ filter. These filters are implemented according to Hogenauer with hardware optimizations, but there are many ways to implement. The $sinc^3$ is also a Hogenauer. It can be bypassed too.

Figure 1.5B is a view of Figure 1.5A, modified to include settled mode selection. When settled mode is selected, control logic 304 asserts control over the serial port to prohibit output of data from the filter(s) until the filter output is fully settled. When the filters are fully settled, the control logic 304 asserts the "settled" signal to the serial port and permits the serial port to transfer output data to the user.

Figure 1.6A shows the register space in the serial port. This port controls the operation of the port and provides an interface to the user. It is an SPI port and is described more in detail hereafter. Many other implementations are possible, too.

Figure 1.6B is a diagram showing a modification of the serial port of Figure 1.6A to include settled mode selection. In this approach, the configuration register 550 includes one or more bits to specify whether settled mode (output of data occurs only

when the filters are fully settled) or unsettled mode (data is output substantially continuously regardless of whether the filter is settled or not) is in effect. In this approach, the user sets the desired settled mode by writing to the mode selection bit(s) of the configuration register over the serial port.

This approach is an alternative to the use of a separate "mode" pin shown in figure 1.1B.

Figure 2.0 is a schematic diagram of a rough buffer used in conjunction with a switched capacitor circuit such as might be found used in conjunction with the delta sigma modulator 120 shown in Figure 1.

A rough buffer amplifier 200 receives a voltage input V_{in} and produces an output, which, when switches IR are closed, will charge capacitor C at an aggressive rate. This permits the capacitor C to approach the input voltage, V_{in}, quickly. Once a capacitor C is charged approximately to the input voltage, the rough buffer is switched out by opening switches IR. At the same time, switches IF are closed permitting the capacitor to enter a fine charge mode in which the V_{in} is applied directly across capacitor C permitting the capacitor to settle very quickly to the value of V_{in}. Once capacitor C is charged to V_{in}, switches IF are opened and switches 2 are closed connecting the charge capacitor C across the input of op-amp 210. A switched capacitor input has input current $CxV_{in}xF$. A rough buffer will provide this current so that the current from the signal source is only $CxV_{error}xF$, where V_{error} is the residue of the voltage error after rough charging. This reduces the loading on the input source and permits greater accuracy.

In the past, a single stage amplifier, such as a folded cascode has been used. This requires high power consumption on the same order as that consumed by the op amp and reduced output swing due to the cascode nature of the circuit. A two-stage amplifier would provide a wider swing and can provide reduced power when compared to a single stage device.

Figure 2.1 is a schematic diagram of a two-stage amplifier. In this illustration, the rough buffer amplifier is shown in more detail in an n-device implementation. This approach uses a first stage amplifier and an n-device output stage. The output response of the two-stage amp shown in Figure 2.1 is shown in Figures 2.2 and 2.3. Considering Figure 2.2, a signal step couples through capacitor C_c to node V2, this turns off device M2, so that the change in V_{out} is only achieved by I_{bias} with a slope of $dV/dt=I_{bias}/C$. The only way to

speed this up is to apply additional power which would increase I_{bias}.

Considering Figure 2.3, a step and input voltage couples through capacitor C_c and pulls up V_2. This turns on device M2 stronger (there is a quadratic relationship between I_d versus V_{gs}) and quickly pulls down node V_{out}. Low quiescent current is required, but there is a large current available for the pull down.

There is still however, a remaining problem. If $V_{out} > V_x$, the amplifier is still slower. If an amplifier of opposite devices (e.g., turn all P devices to N devices and all N devices to P devices) is used, the behavior is good for $V_{out} > V_x$ but is slower for $V_x > V_{out}$. This is illustrated in Figure 2.4.

Figure 2.5 shows a two-stage amplifier using a comparator to select which output stage to utilize in accordance with the invention.

As shown in Figure 2.5, two different second stage amplifiers 220 and 230 are utilized. Second stage amp 220 is implemented using n-devices and second stage amp 230 is implemented using p-devices. Two separate paths are utilized selectively for receiving the output of the first stage amplifier 200. One path is selected when the useN switches are closed and the other is selected when the useP switches are closed. A decision as to which path to utilize is made using comparator 240, the output of which is determined by the relationship between V_N and V_x. A decision is made during phase 2 which output to select during the phase 1 rough charge. The selection is made such that the fastest response path for a given relationship between V_n and V_x is selected.

The input to the first stage amplifier 200 can be advantageously an input stage that uses rail to rail input. These are known from the prior art. Further, one may use chopper stabilization to remove the offset from the voltage V_{error}.

Figures 2.6, 2.7 and 2.8 show the transfer function, a step response and the output to the step response of the two-stage amplifier shown in Figure 2.5, respectively. Specifically, Figure 2.6 shows relationships between V_x and V_{IN}. Figure 2.7 shows alternating rough charge fine charge phases and shows the state of the output of the comparator useP. Finally, Figure 2.8 shows the output V_{out} during the various stages of operation.

The net result of this implementation is that there is always a fast response to a change in input signal regardless of the polarity of the input signal.

Figure 3.1 is a block diagram of a serial multiplier of Figure 1.5 implementing the encoding scheme shown in Figures 3.2 and 3.3 to achieve multiplication. As shown in

Figure 3.1, a gain word is loaded into shift register 410. The encoding scheme is discussed more in U.S. Patent 3,691,359 to Dell et al. However, Dell et al. do not show the architecture of Figure 3.1, merging in the final pass and two's compliment multiplication. This gain word represents the gain setting specified for the particular channel being processed. The stored gain word is supplied to encoder 411 where a table corresponding to Figure 3.2 is derived from the gain word stored. The incoming serial bits of the bit to be multiplied are examined two at a time to determine whether 0, B, -B or 2B processing is required in accordance with the table in Figure 3.2. The selected output is then passed through 4-1 mux 413 to multiplexer 414 where either the output from the 4-1 mux 413 is applied to adder 415 and one output from adder 415 may be selectively recirculated as part of a carry ripple operation to a second input of mux 414, thus saving a row of adders. The output of the summed output from adder 415 is applied into a sum register which can be selectively recirculated to produce the ultimate product at the output of the multiplier. A counter 418 is initiated at the beginning of multiplication and issues a mult_done output when the multiplication has been completed.

Figure 3.4 and Figure 3.5 show examples of multiplication in accordance with one aspect of the invention. In example 1 shown in Figure 3.4, two numbers A=2 and B=5 are to be multiplied together. A is represented in binary as 000010 and B is represented in binary as 0101. Multiplication in accordance with the invention differs from prior art multipliers in several respects. In a first respect, the multiplier A, is analyzed two bits at a time instead of one. Considering first the two at least significant bits of the multiplier A, they are "10." This translates to a multiplication of B by the number 2. 2B results in a shift to the left of the numeral B resulting in the four least significant digits of 1010. Each of the more significant pairs of bits in multiplier A are "00." Each of these results in a 0 multiplication of B resulting in 0. Therefore the least four significant bits of the product 0xB will be 0000. As can be seen in example 1, a pair of 1's precedes each of the products resulting from the pair wise multiplication of B. In addition, a single "1" occurs for the first single bit position for which no multiplication was done. This permits proper tracking of the signed bit during execution of the multiplication. Thus the product 2B is preceded by two 1's or in other words 111010 represents 2B where the first two 1's are used for tracking the signed bit and the last four bits are the product of 2xB or 10 (decimal). The 2 bit examination of digits of the multiplier result in a two bit shift for each pair of bits examined.

This results then in a four layer addition shown in example 1. When all of these binary numbers are added, the correct results shows at the bottom, namely 10, or "0000001010."

Example 2 described in Figure 3.5 is the same as example 1 except that the multiplier is a negative number, namely -2. The representation of a negative number is done using a two's complement of the positive number. In other words, -2 is equal to the two's complement of 2 or 111110. Again, considering the two lest significant bits of the multiplier A, namely 10, one will multiply the number B by the number 2 which produces the same result that occurred in the previous example. Each of the next two pairs of bits is 11. The first 11 has a carry in of 0. The remaining value A-B comes from table 3 of Figure 3.5. The next 11 has a carry in of 1 resulting in a value of zero from table 3 preceded by a sign and sign extension bits "11" in a 3B representation. 3B = 4B - B.

The family of chips shown in Figure 1 is designed to support a technique for performing data conversion which greatly increases the use of calibration registers.

This is accomplished through use of a group of setup registers, a configuring register, offset and gain calibration registers, and a serial port command structure.

The setup registers contain logical channels to be converted. Each logical channel contains bits which are used to specify conversion options such as conversion rates, gain selection, unipolar/bipolar input span, selection of the physical channel to be converted, etc.

The integrated circuits provide offset and chain calibration registers for each physical channel. These registers hold calibration results and are also writable by the user contained dedicated offset and gain calibration registers for each physical channel. This dedicated pair of registers results into a non-optimal utilization of silicon area, as the user who intends to connect only a subset of available channels and doesn't get to use the registers dedicated to the unused channels. The approach according to the invention rectifies the problem by allowing the user to assign any register to any physical channel.

Figure 4.1 is a register diagram of the serial port 140 of figure 1 showing calibration and SRAM/control logic 150 of Figure 1.1.

Figure 4.2 is a block diagram of a serial multiplier of Figure 3.6 implementing the encoding scheme shown in Figures 4.1.0 and 4.1.1 to achieve multiplication. The data structure shown in Figures 4.2 and 4.3 describes how to access the offset and gain registers through serial port.

For example, if a command issued is 21 (Hex), it translates to writing offset register

3. (Offset 3 in Figure 9) similarly 12 (Hex) translates to writing gain register 2 (Gain 2 in Figure 1). This way the user can read or write to any offset/gain register through serial port. These registers are also written during calibration. They get used during normal conversion to adjust offset and gain of the converter.

Figure 4.3 shows more of the serial port command structure shown on Figure 4.2.

The following command byte structure describes the conversion commands.

Consider the example of Figure 4.4. Discussion of the corresponding Figure. In the Example shown on Figure 4.4, the first two bits (those shown to the left of the bits stream shown in the Example) indicate that the data structure represents a command and that the command specifies performing a fully settled single conversion. The next three bits however are pointer bits to the channel set up register. In this case, the bits "001" point to set up register number one. The first two bits of set up register number 1 are pointers to the physical channel address, in this case 11. The physical channel address then identifies the gain and off set registers as well since, in this implementation, there is a dedicated relationship between them.

The command 88 (Hex) means, convert using setup register 2. If setup register 2 contains physical channel information as depicted (79), it means that physical channel 4 should be converted using offset register 4 and gain register 4.

As mentioned before, this results in a non-optimal use of registers. If physical channel addresses can be delinked from the calibration register address, we can achieve independent control of these registers.

One way to achieve the desired effect is by using a bit of configuration register and more bits of setup registers as shown in Figure 4.5.

Here the command 88 (Hex), points to setup register 2, with physical channel 4 to be converted. If configuration bit select is high, the address of the gain and offset registers now comes from the two LSB bits of setup register being pointed to (setup register 2 in this example). Thus any physical channel can be combined with any offset/gain register pair. In the above example, physical channel 3 is to be converted using offset-register 3 and gain register 3. Note that the offset and gain registers are used in pairs so far. To offer total control over the choice of offset or gain register, more bits of setup registers are needed as shown in Figure 4.6.

Returning to Figure 1.1, when verifying the performance of an integrated circuit chip, such as shown in Figure 1, it is desirable to know whether or not the 1/f performance of components, such as the programmable instrumentation amplifier 110, is within specifications. To actually measure the 1/f noise at a frequency of, for example, 0.1Hz requires approximately 10 seconds of measurement time. Such a long testing interval is inconsistent with a desire to mass produce integrated circuit chips in high volumes.

Figure 5.1 is a flow chart of a process for verifying that 1/f noise is within specifications in a short internal even if very low frequencies are of interest. Essentially the approach used uses a determination that chopper stabilization is working appropriately as a substitute for actually testing 1/f noise. If chopper stabilization is working properly, then most of the 1/f noise would be eliminated.

Turning to Figure 5.1, a test is conducted by introducing a value of intentional offset inside the chopper stabilized amplifier greater than the expected random variation in amplifier input offset (800). A check is made whether the output offset is within the range of expected output offset which would occur if chopper amplification were working properly (810). If the amount of offset is within that range (810-Y), the 1/f noise is assumed to be eliminated within specification (830). If it is not (810-N), the 1/f noise is presumed to exceed specifications and the part is rejected (820).

Figure 6.1 is a partial schematic, partial block diagram of the integrated circuit of Figure 1 used to measure the output of a thermocouple. A thermocouple 900 is connected to inputs ain1+ and ain1-. A cold junction 901 produces a signal equivalent to a thermocouple at room temperature and that signal is applied across inputs ain2+ and ain2-. The signals from each of these two sources can be processed and provided to the serial data interface 902 which connects with a serial port on the chip to provide the user access to the temperature information resulting from the signal processing done on the chip. Exemplary power and biasing information is shown in the drawing.

Figure 6.2 is a partial schematic, partial block diagram of the integrated circuit of Figure 1 used to measure the output of a bridge transducer.

A bridge transducer might be used in a weigh scale and might have an output signal of less than 5mV. The mechanical elements of a weigh scale have a temperature coefficient. It is required to measure the temperature of the system. This is often done using a 5th resistor that is connected to either the positive or negative supply. The

resolution requirement for this measurement is such that amplification before conversion is not necessary. It is a very desirable feature in a weigh scale application to be able to convert a rail/rail input signal without external components. The addition of a bypass as a unity gain mode to the switched capacitor based ADC with rail to rail input range allows the easy implementation of this measurement. The real goal is low input current on the switched capacitor adc. It is required, when doing this, to provide active rough buffering so that the switched capacitor input currents described earlier, which would be drawn through the resistors, do not corrupt the precision of the measurement. In this application, it is also desirable to use rough buffering and reduced input currents on the reference. Alternatively a rough charge buffer could be replaced with a regular buffer circuit that is not bypassed during a fine charge phase. This allows the use of resistive voltage division on the reference (for better SNR of the measurement) or protection resistors in place.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims and their equivalents.

Docket No. 2005-0154

What is claimed is:

1. An integrated circuit comprising:

a. an analog to digital converter;

b. an FIR filter; and

c. an output mechanism selectively providing either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

2. The integrated circuit of claim 1 in which the output mechanism comprises an external pin on the integrated circuit to which a user can apply a control signal to control the selection of fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

3. The integrated circuit of claim 1 in which the output mechanism comprises an one or more bits on a register of the integrated circuit to which a user can set to control the selection of fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

4. The integrated circuit of claim 3 in which said one or more bits on a register of the integrated circuit are set over a serial port interface.

5. The integrated circuit of claim 1 in which the analog to digital converter is a delta sigma modulator.

6. The integrated circuit of claim 1 in which the FIR filter is a decimation filter.

7. A method of designing an integrated circuit having an FIR filter, comprising the step of providing an mechanism to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

8. A method of fabricating an integrated circuit having an FIR filter, comprising the step of providing an mechanism to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

ABSTRACT

In a signal processing integrated circuit having an analog to digital converter and a digital filter having a plurality of taps separated in time, when starting a conversion after a reset or a change of input channel, the filter will have an incomplete set of input data as the delayed inputs to an output calculation are all zero from the reset operation. After reset, during the time that data are filling up the filter pipeline, the calculation of an output value will give a result that holds information about the input, but does not present the data with the same scaling and frequency content as the fully settled filter. The integrated circuit selectively provides two modes, on that provides only fully settled data from the filter or and another that provides all data from the filter, including unsettled data. Knowledge about the filter coefficients can be utilized by a user or user process to extract information about the input from the unsettled data.

Express Mail No. EV 335 052 704 US

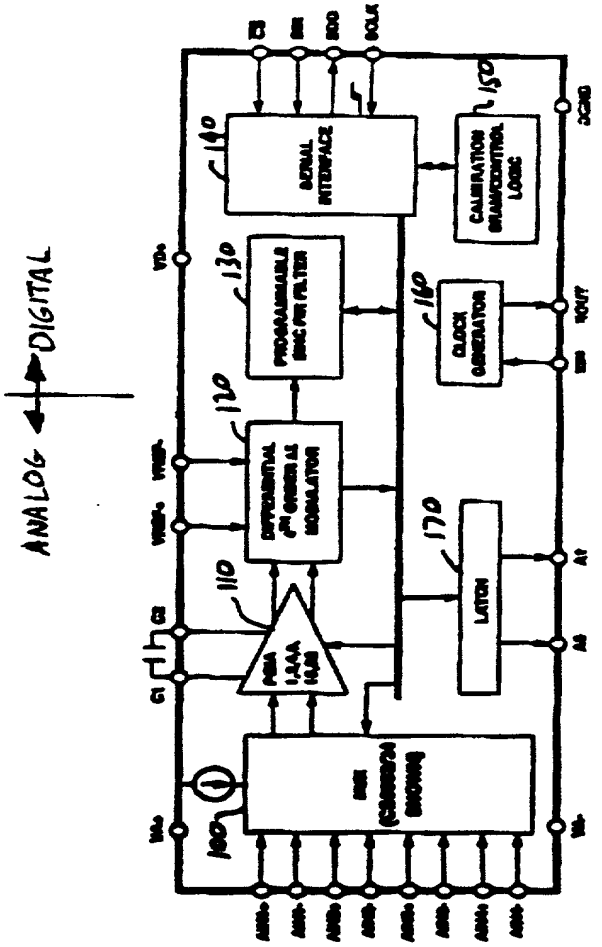
ANALOG
DIGITAL
SERIAL INTERFACE
CALIBRATION SYNCHRONIZATION LOGIC
PROGRAMMABLE SINC FIR FILTER
CLOCK GENERATION
DIFFERENTIAL ΔΣ MODULATOR
PGIA
LATCH
110
120
130
140
150
160
170

FIGURE 1.1A

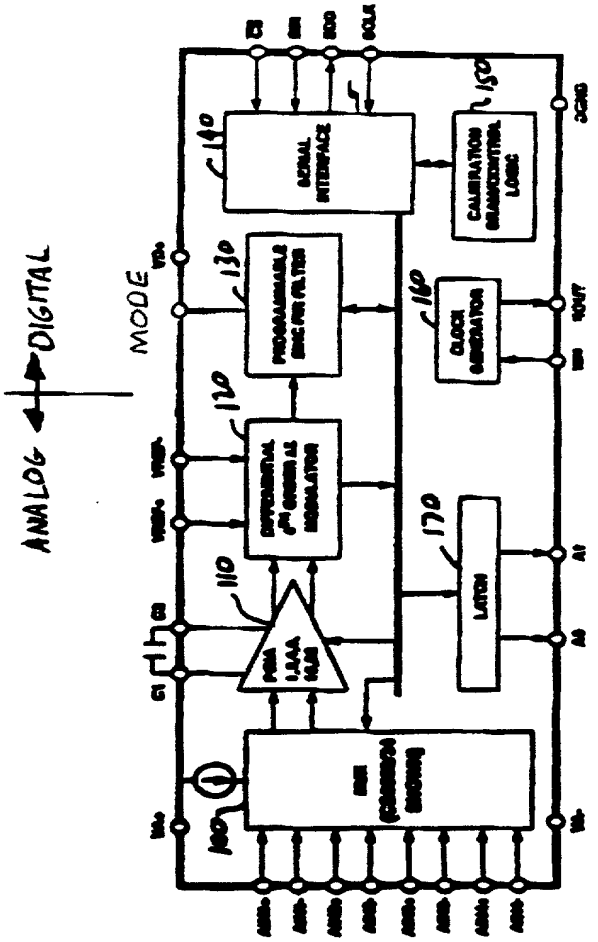

FIGURE 1.1B

05/26/00 "10:56:50

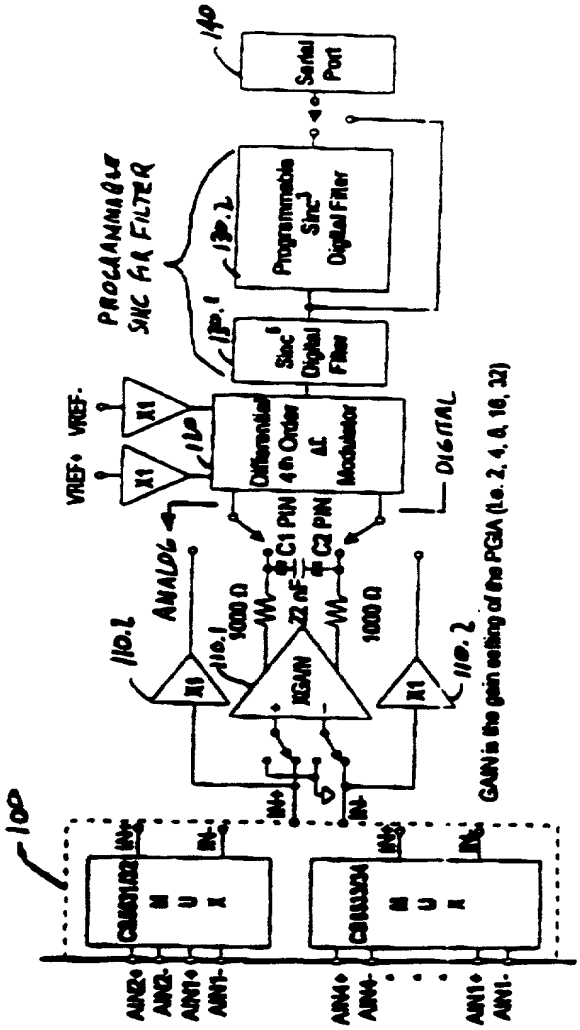
140
Serial Port
PROGRAMMABLE SINC FIR FILTER
130.2
Programmable Sinc³ Digital Filter
130.1
Sinc¹ Digital Filter
VREF+ VREF-
X1
X1
110
Differential 4th Order ΔΣ Modulator
DIGITAL
C1 PIN
C2 PIN
ANALOG
110.1
110.2
X8
1000 Ω
22 nF
1000 Ω
XGAIN
X1
IN+
IN-
100
MUX
MUX
AIN2+
AIN2-
AIN1+
AIN1-
AIN4+
AIN4-
AIN1+
AIN1-
GAIN is the gain setting of the PGIA (i.e. 2, 4, 8, 16, 32)

FIGURE 1.2A

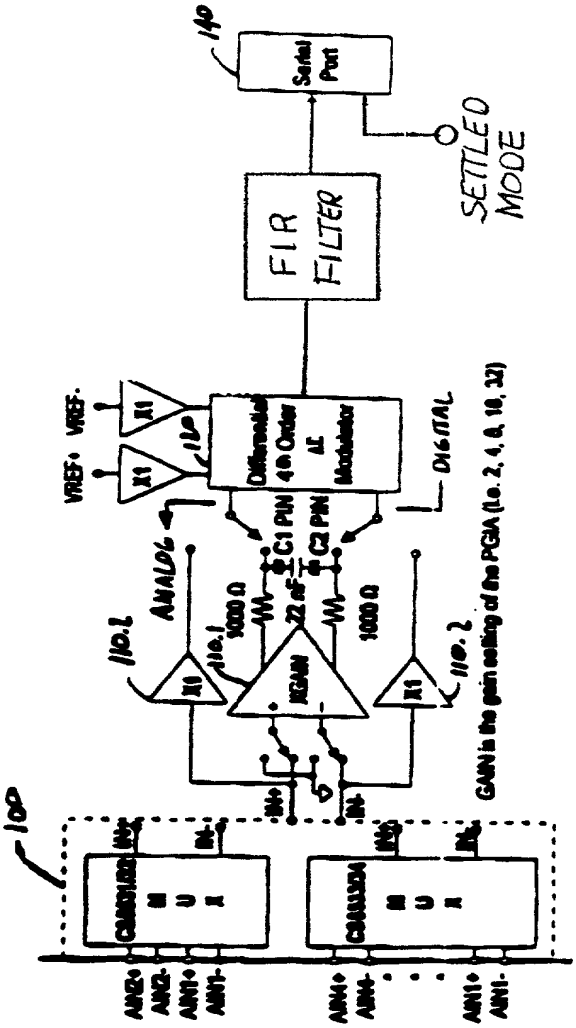
140
Serial Port
SETTLED MODE
FIR FILTER
Differential 4th Order ΔΣ Modulator
DIGITAL
VREF+ VREF-
X1
X1
120
C1 PIN
C2 PIN
ANALOG
110.1
110.2
1000 Ω
1000 Ω
22 nF
PGAIN
X1
X1
GAIN is the gain setting of the PGIA (i.e. 2, 4, 8, 16, 32)
100
MUX
MUX
AIN2+
AIN2-
AIN1+
AIN1-
AIN4+
AIN4-
AIN1+
AIN1-

FIGURE 1.2 B

0052608 "40,456,960

FIG 1.26

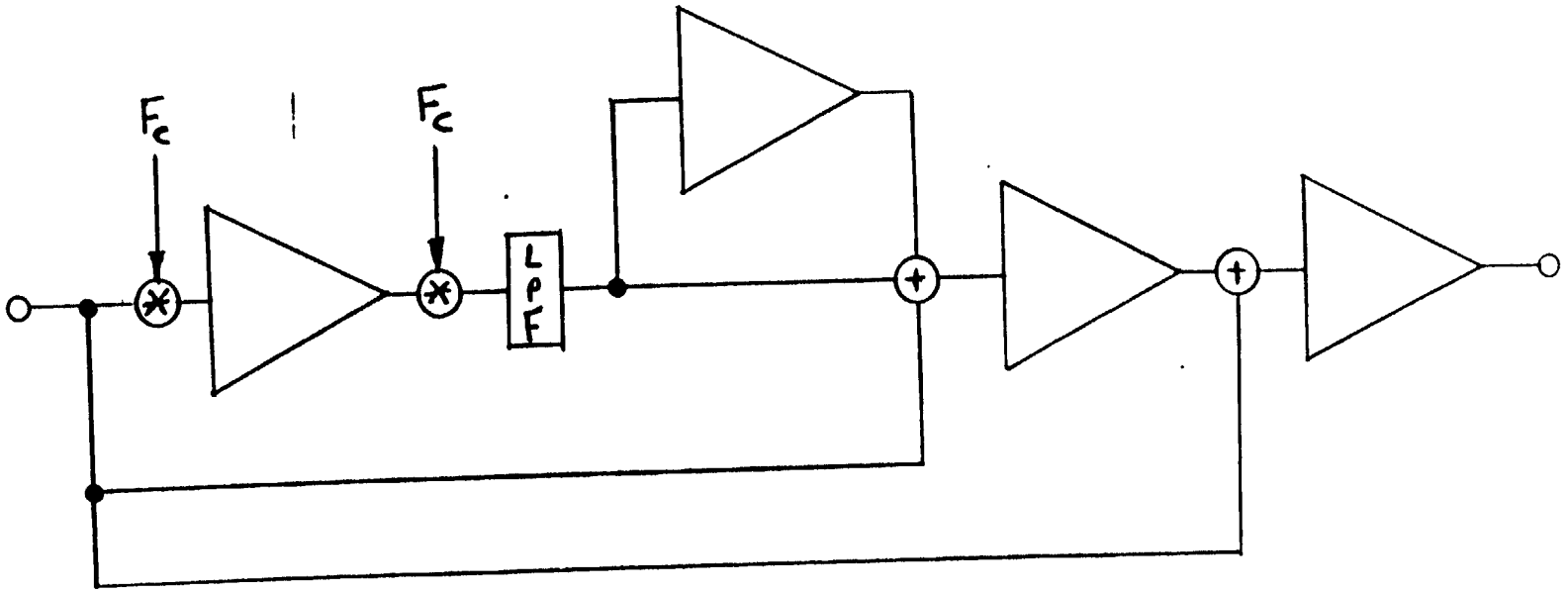

FIGURE 1.3

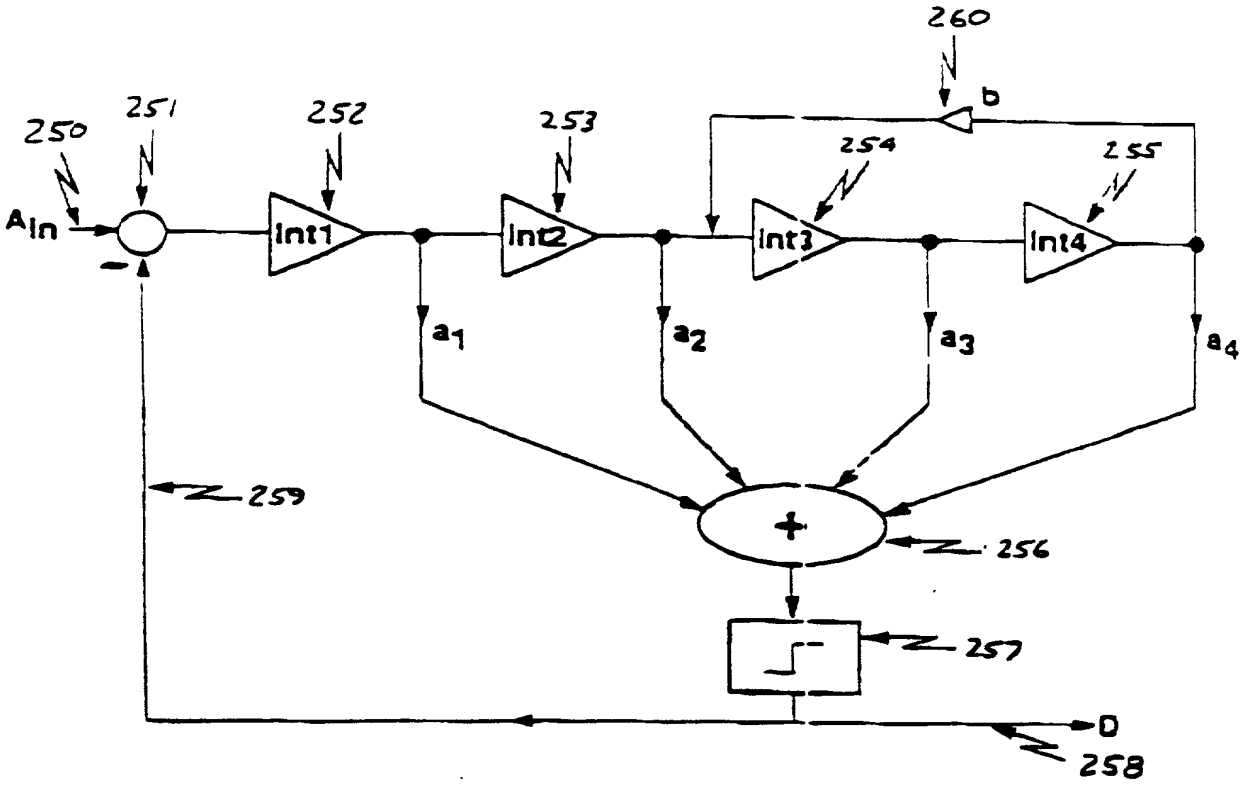
260
b
250
251
252
253
254
255
Ain
Int1
Int2
Int3
Int4
a1
a2
a3
a4
259
+
256
257
D
258

Figure 1.4

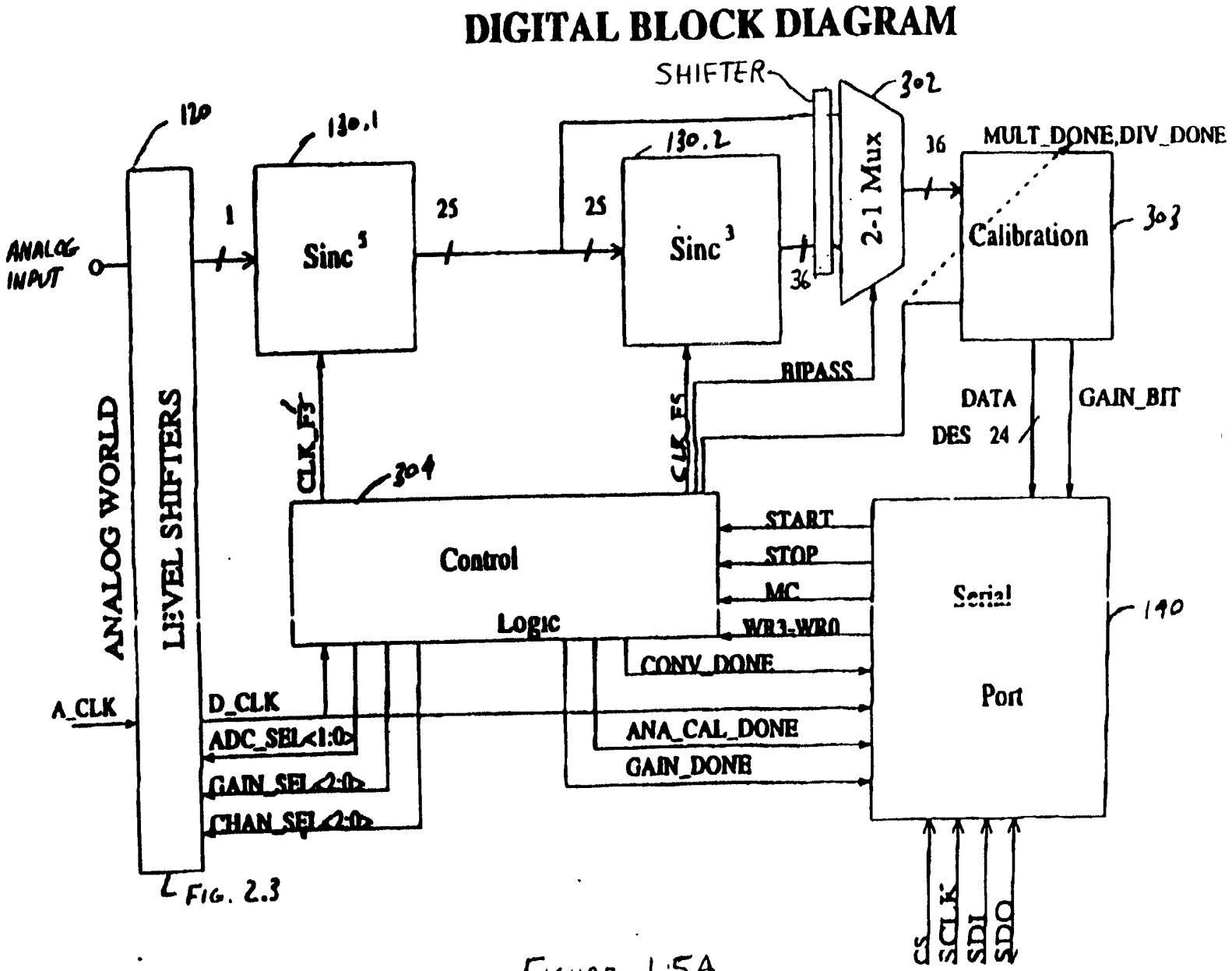

FIG. 2.3

FIGURE 1.5A

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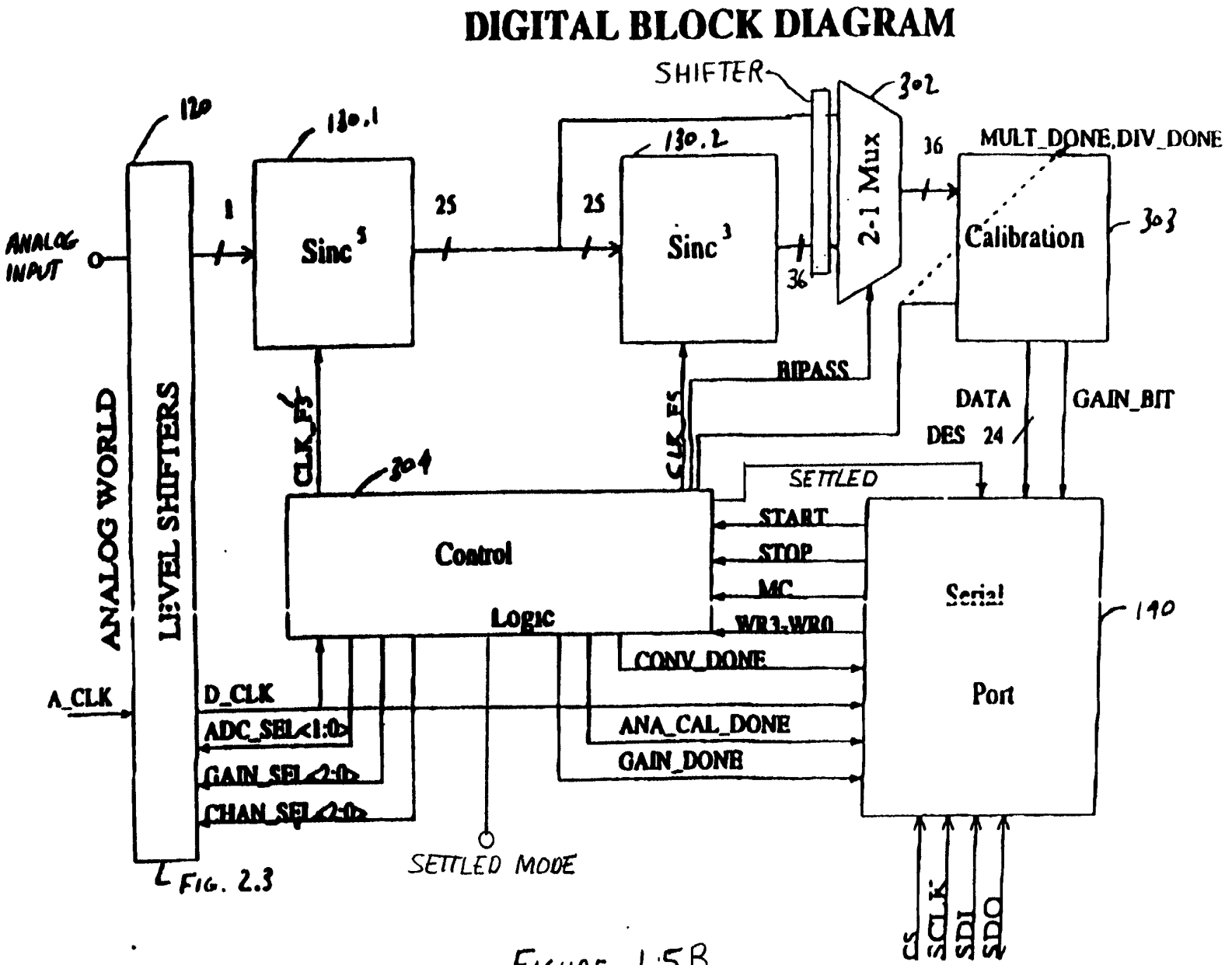

FIGURE 1.5B

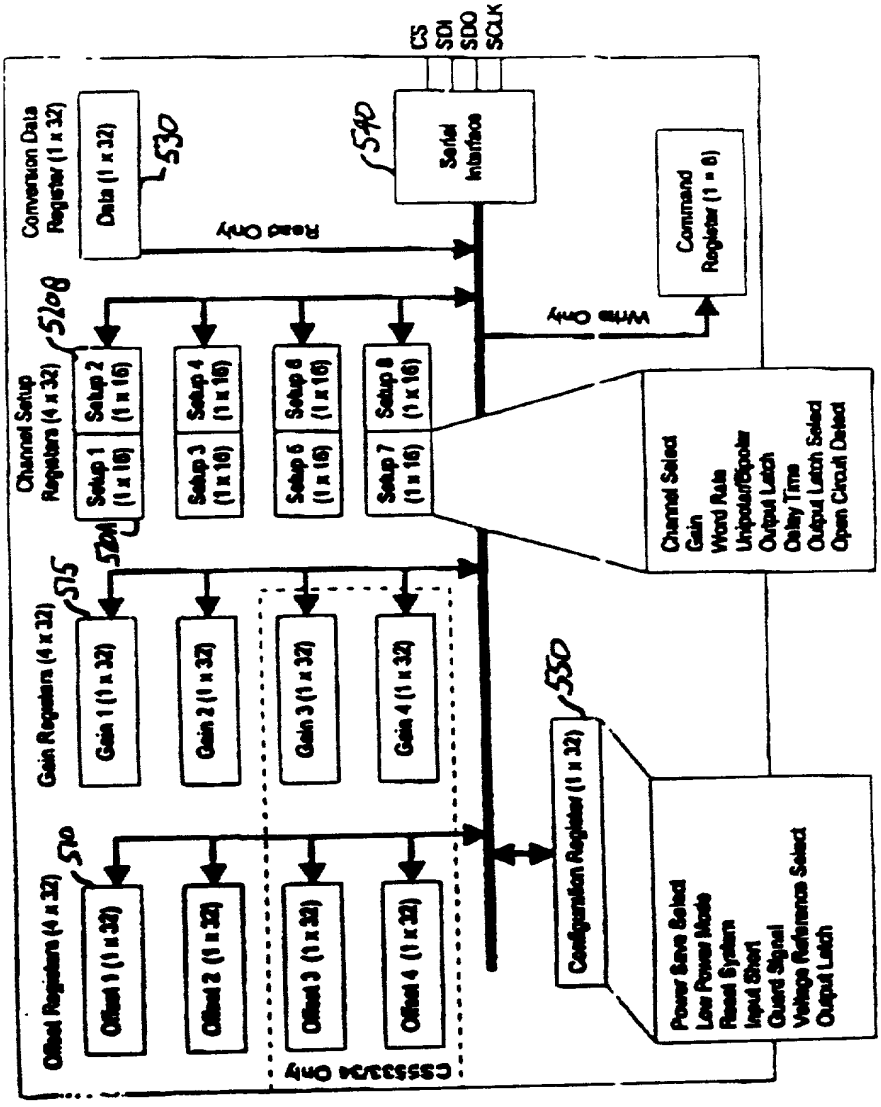
CS
SDI
SDO
SCLK
Conversion Data Register (1 x 32)
Data (1 x 32)
530
Read Only
540
Serial Interface
Command Register (1 = 8)
Write Only
Channel Setup Registers (4 x 32)
520a
Setup 1 (1 x 16)
Setup 2 (1 x 16)
Setup 3 (1 x 16)
Setup 4 (1 x 16)
Setup 5 (1 x 16)
Setup 6 (1 x 16)
Setup 7 (1 x 16)
Setup 8 (1 x 16)
520n
Channel Select
Gain
Word Rate
Unipolar/Bipolar
Output Latch
Delay Time
Output Latch Select
Open Circuit Detect
515
Gain Registers (4 x 32)
Gain 1 (1 x 32)
Gain 2 (1 x 32)
Gain 3 (1 x 32)
Gain 4 (1 x 32)
530
Configuration Register (1 x 32)
Power Save Select
Low Power Mode
Reset System
Input Short
Guard Signal
Voltage Reference Select
Output Latch
510
Offset Registers (4 x 32)
Offset 1 (1 x 32)
Offset 2 (1 x 32)
Offset 3 (1 x 32)
Offset 4 (1 x 32)
CS5532/34 Only

FIGURE 1.6A

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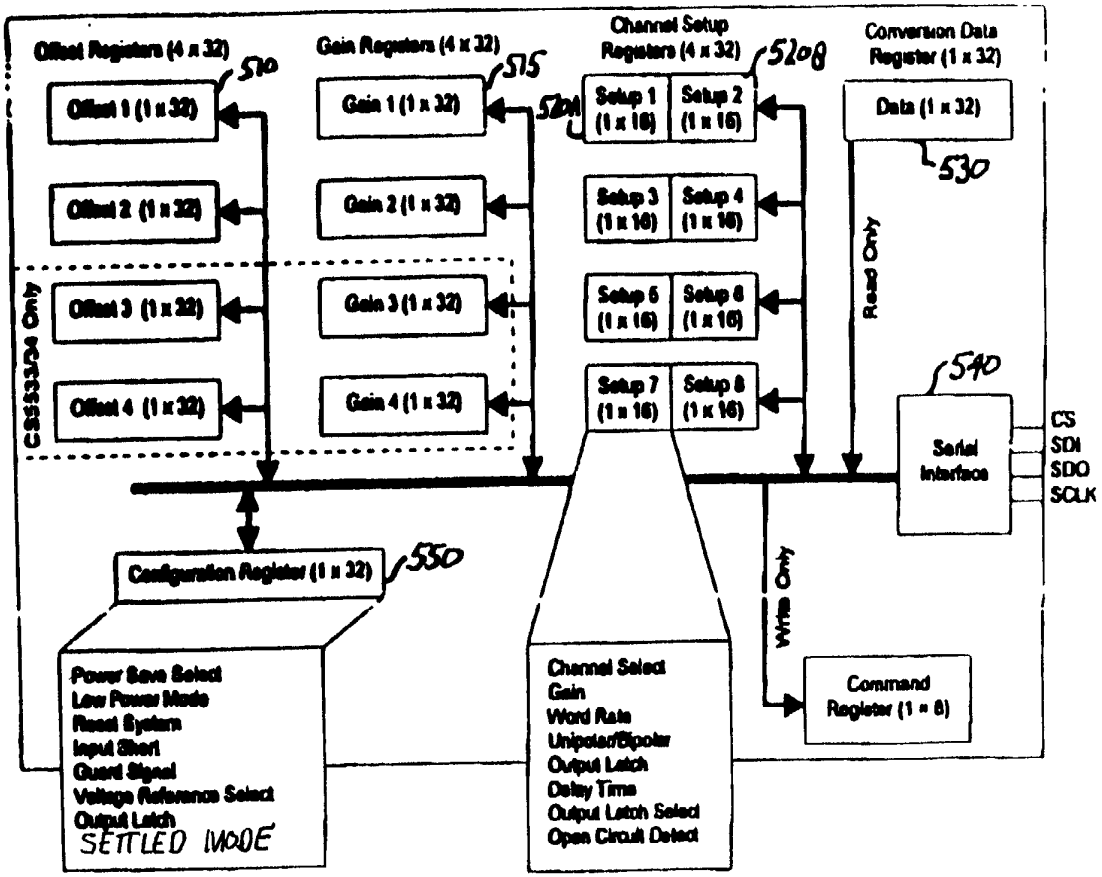


FIGURE 1.6B

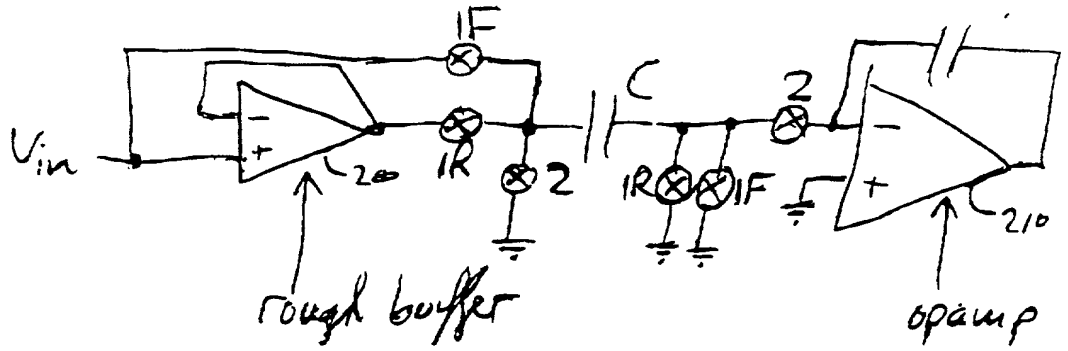


FIGURE 2.0

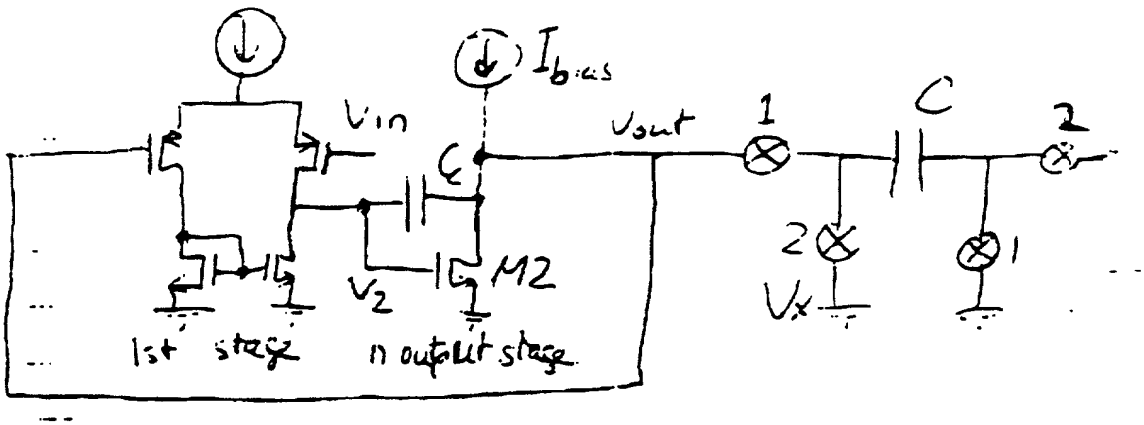


FIGURE 2.1

V_{IN} = CONSTANT

$V_{OUT} > V_X$

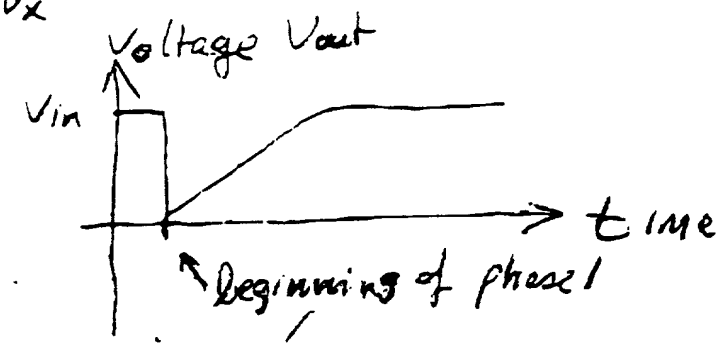


FIGURE 2.2

V_{IN} = CONSTANT

$V_{OUT} < V_X$

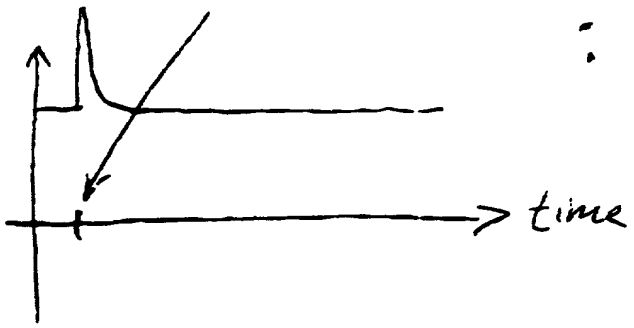


FIGURE 2.3

05/20/04 THU 15:56 [TX/RX NO 6130]

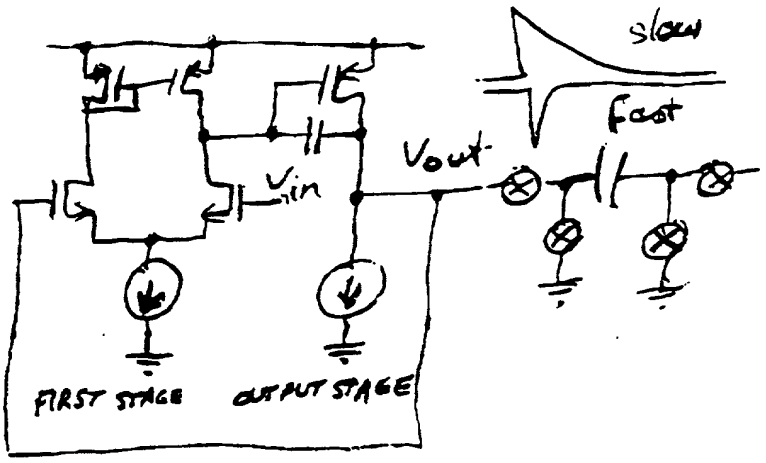


FIGURE 2.4

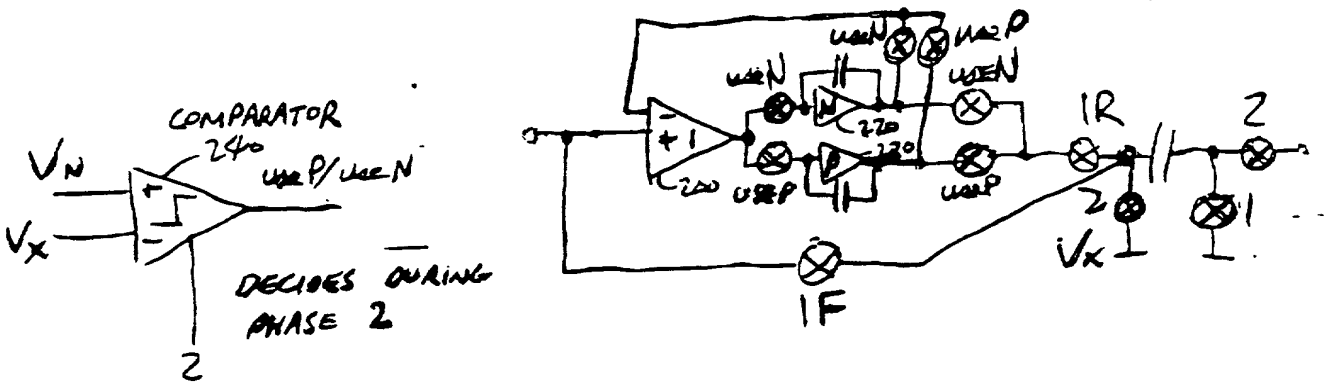
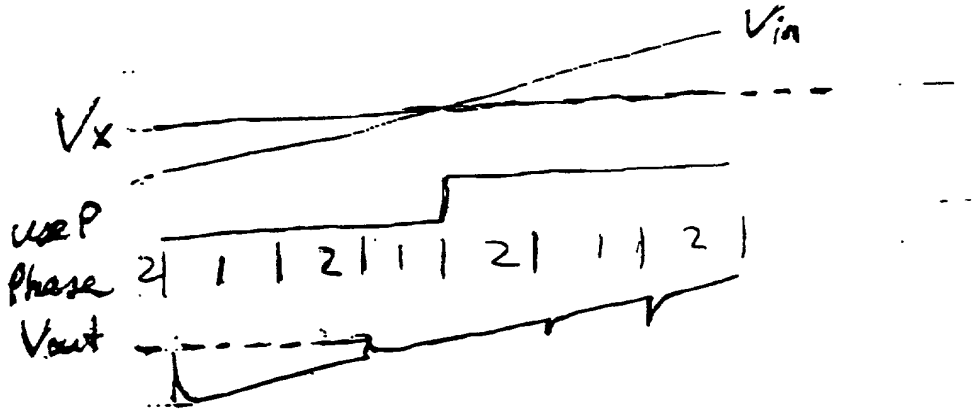

COMPARATOR
240
V_N
V_X
ϕ_{2P}/ϕ_{2N}
DECIDES DURING PHASE 2
2
ϕ_{2N}
ϕ_{2P}
+1
220
230
ϕ_{2P}
ϕ_{2N}
ϕ_{2P}
ϕ_{2N}
1R
2
2
1
V_X
1F

FIGURE 2.5

FIGURE 2.6

FIGURE 2.7

FIGURE 2.8



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MULTIPLIER ARCHITECTURE

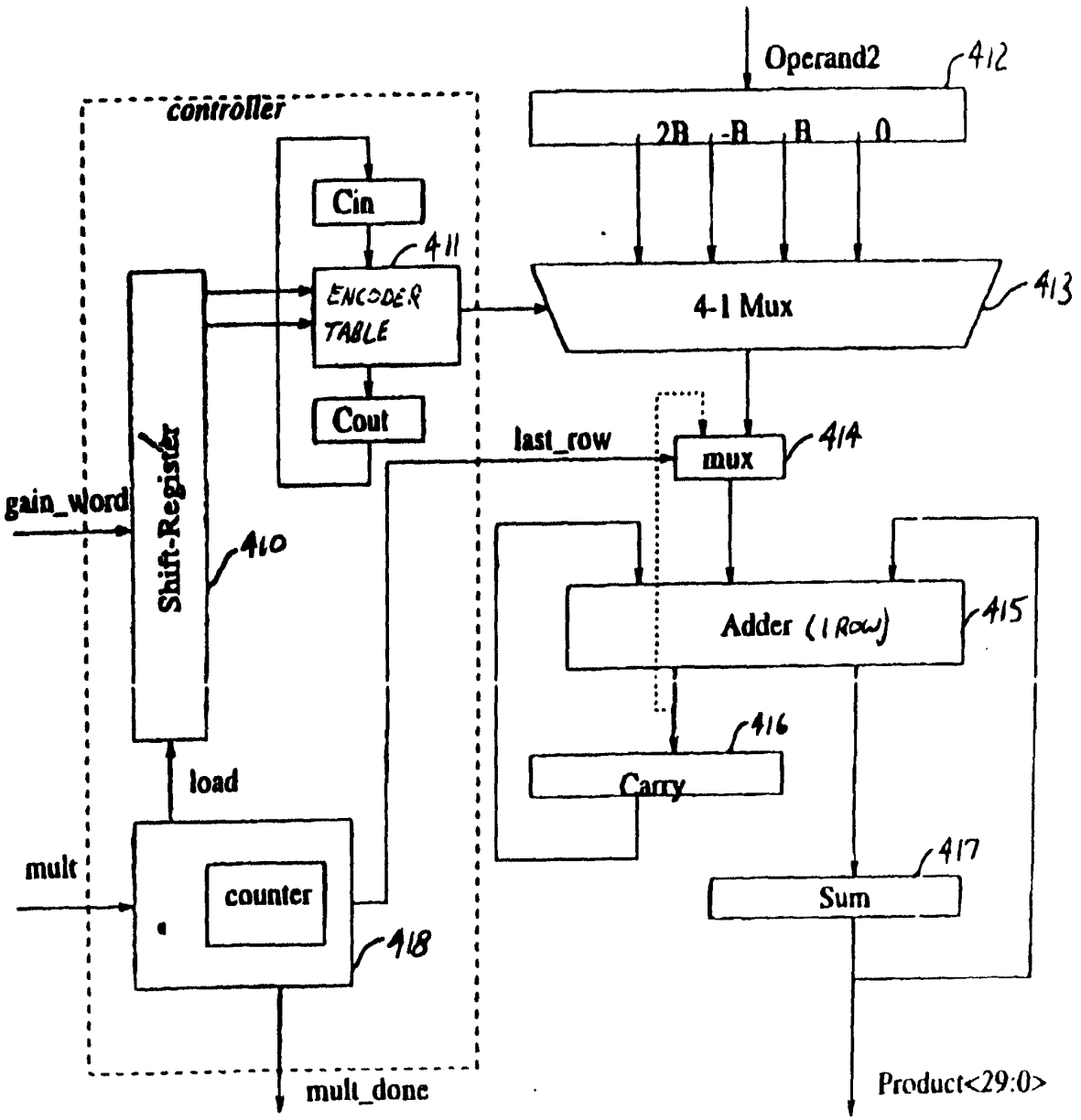

FIGURE 3.1

NOV 12 99 07:24a David L Stewart 703 441-2025 P 27

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Multiplication

FIGURE 3.2
(PRIOR ART)

Table 2: Encoding Scheme Proposed

A_{i+1}	A_i	Operation
0	0	$R_i = R_{i-1}/4$
0	1	$R_i = (R_{i-1} + B)/4$
1	0	$R_i = (R_{i-1} + 2B)/4$
1	1	$R_i = (R_{i-1} + 3B)/4$

FIGURE 3.3
(PRIOR ART)

Table 3: Carry Propagate Encoding Scheme

C_{in}	A_{i+1}	A_i	Operation	C_{out}
0	0	0	$R_i = R_{i-1}/4$	0
0	0	1	$R_i = (R_{i-1} + B)/4$	0
0	1	0	$R_i = (R_{i-1} + 2B)/4$	0
0	1	1	$R_i = (R_{i-1} - B)/4$	1
1	0	0	$R_i = (R_{i-1} + B)/4$	0
1	0	1	$R_i = (R_{i-1} + 2B)/4$	0
1	1	0	$R_i = (R_{i-1} - B)/4$	0
1	1	1	$R_i = (R_{i-1})/4$	1

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Multiplication

FIGURE 3.4

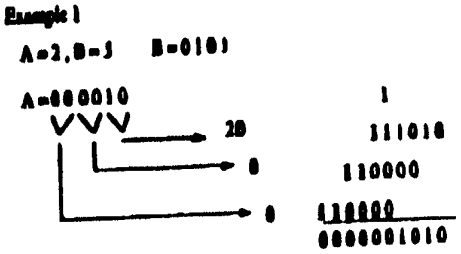
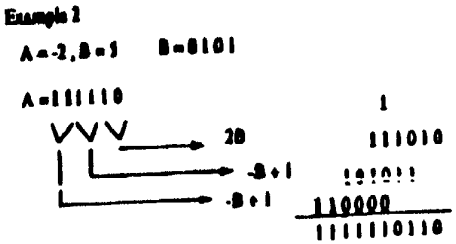


FIGURE 3.5



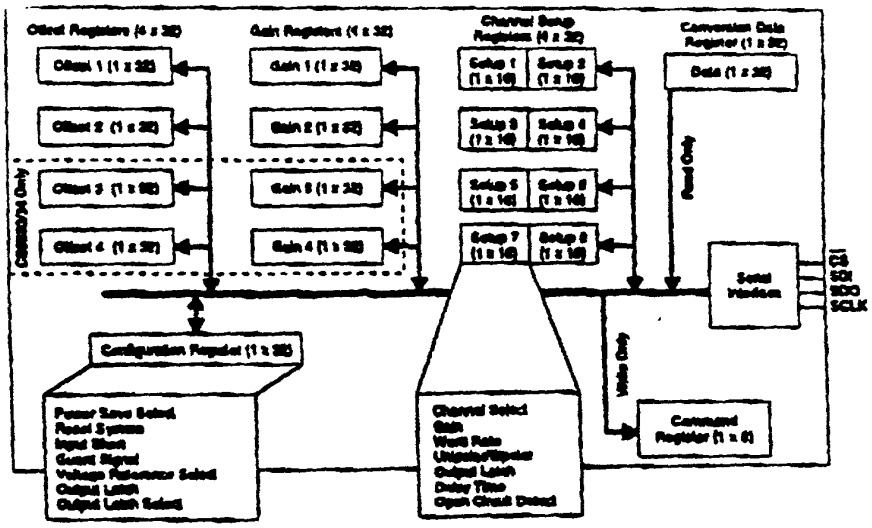

Offset Registers (4 x 32)
Gain Registers (4 x 32)
Channel Setup Registers (8 x 32)
Conversion Data Register (1 x 32)
Offset 1 (1 x 32)
Offset 2 (1 x 32)
Offset 3 (1 x 32)
Offset 4 (1 x 32)
Gain 1 (1 x 32)
Gain 2 (1 x 32)
Gain 3 (1 x 32)
Gain 4 (1 x 32)
Setup 1 (1 x 16)
Setup 2 (1 x 16)
Setup 3 (1 x 16)
Setup 4 (1 x 16)
Setup 5 (1 x 16)
Setup 6 (1 x 16)
Setup 7 (1 x 16)
Setup 8 (1 x 16)
Data (1 x 32)
Read Only
Calibration Only
Serial Interface
SDI
SDO
SCLK
Configuration Register (1 x 32)
Power Save Select
Reset System
Input Short
Guard Signal
Voltage Reference Select
Output Latch
Output Latch Select
Channel Select
Gain
Word Rate
Unipolar/Bipolar
Output Latch
Delay Time
Open Circuit Detect
Write Only
Command Register (1 x 8)

FIGURE 4.1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/$\overline{W}$	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	Must be logic 0 for these commands.
		1	These commands are invalid if this bit is logic 1.
D6	Access Registers as Arrays, ARA	0	Ignore this function.
		1	Access the respective registers, offset, gain, or channel-setup, as an array of registers. The particular registers accessed are determined by the RS bits. The registers are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0	00	CS1-CS0 provide the address of one of the two (four for CS5533/34) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.
		01	
		10	
		11	
D3	Read/$\overline{\text{Write}}$, R/$\overline{W}$	0	Write to selected register.
		1	Read from selected register.
D2-D0	Register Select Bit, RSB3-RSB0	000	Reserved
		001	Offset Register
		010	Gain Register
		011	Configuration Register
		100	Conversion Data Register (Read Only)
		101	Channel-Setup Registers
		110	Reserved
		111	Reserved

FIGURE 4.2

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	These commands are invalid if this bit is logic 0.
		1	Must be logic 1 for these commands.
D6	Multiple Conversions, MC	0	Perform fully settled single conversions.
		1	Perform conversions continuously.
D5-D3	Channel-Setup Register Pointer Bits, CSRP	000 ... 111	These bits are used as pointers to the Channel-Setup registers. Either a single conversion or continuous conversions are performed on the channel setup register pointed to by these bits.
D2-D0	Conversion/Calibration Bits, CC2-CC0	000	Normal Conversion
		001	Self-Offset Calibration
		010	Self-Gain Calibration
		011	Reserved
		100	Reserved
		101	System-Offset Calibration
		110	System-Gain Calibration
		111	Reserved

FIGURE 4.3

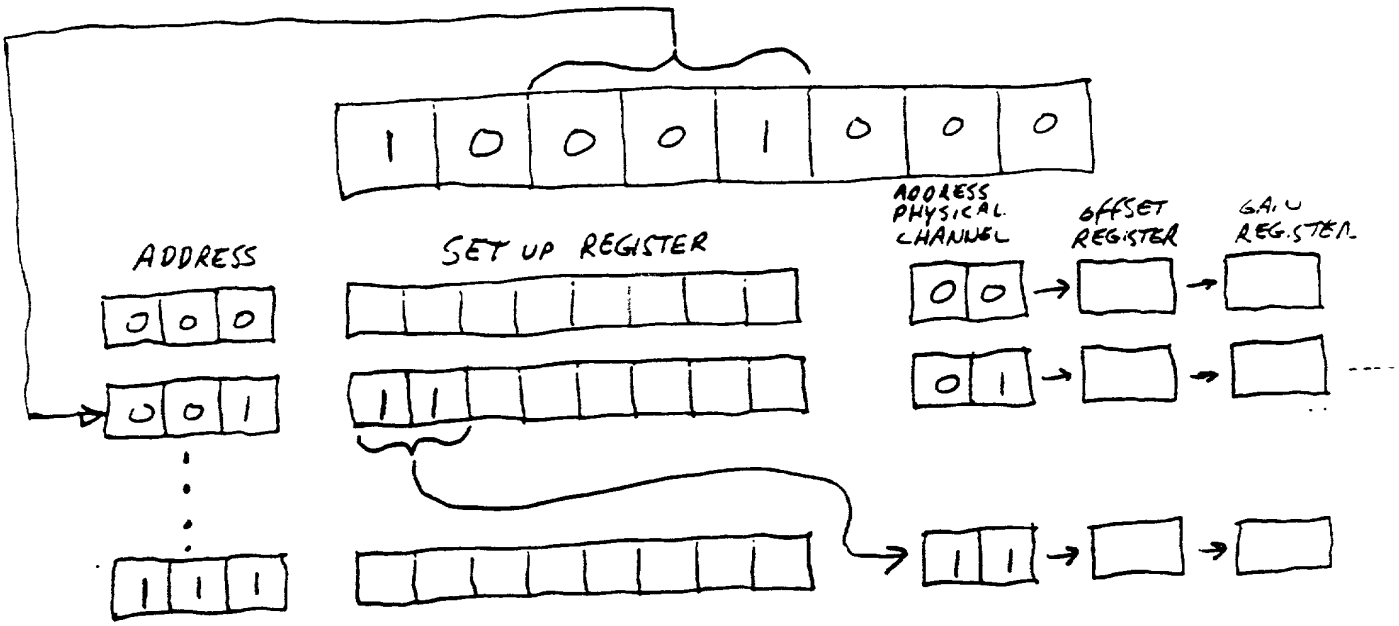

1 0 0 0 1 0 0 0
ADDRESS
SET UP REGISTER
ADDRESS PHYSICAL CHANNEL
OFFSET REGISTER
G.A.U REG.STER.
0 0 0
0 0 1
1 1 1
0 0
0 1
1 1

FIGURE 4.4

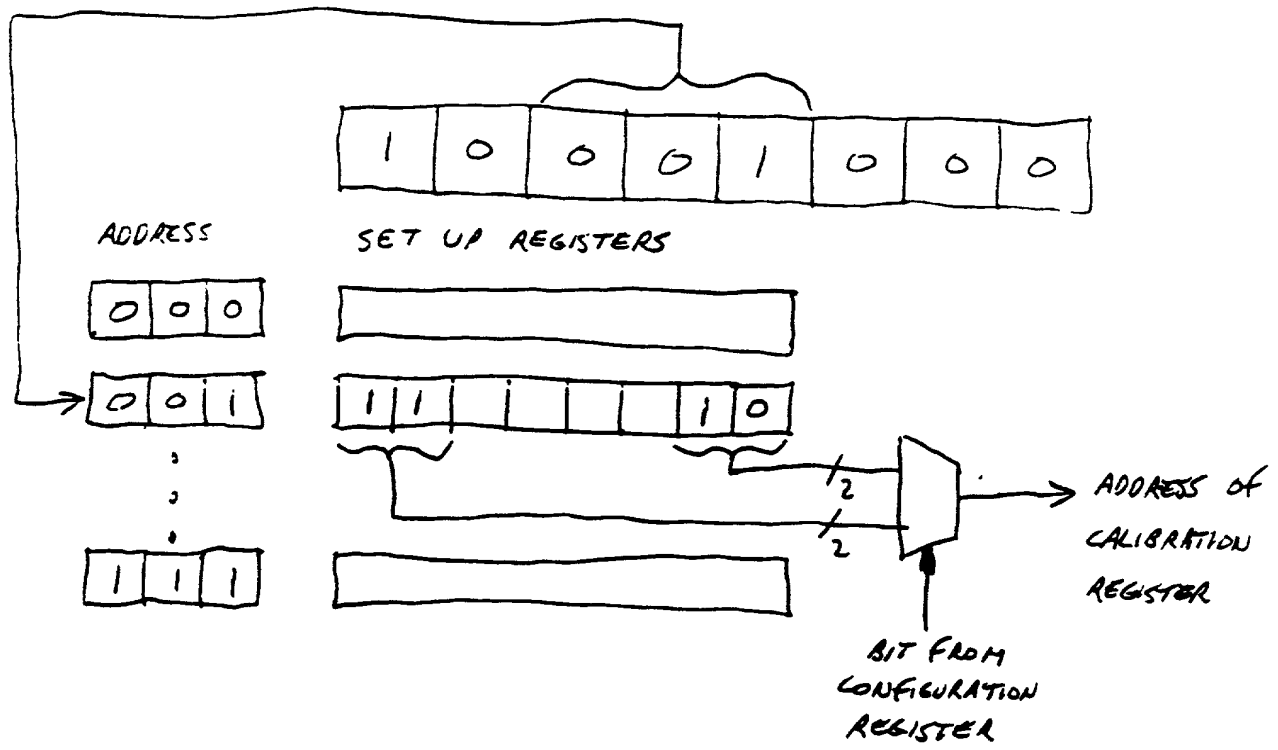

1 0 0 0 1 0 0 0
ADDRESS
SET UP REGISTERS
0 0 0
0 0 1
1 1 1
1 1 1 1 1 1 1 0
2
2
ADDRESS OF CALIBRATION REGISTER
BIT FROM CONFIGURATION REGISTER

FIGURE 4.5

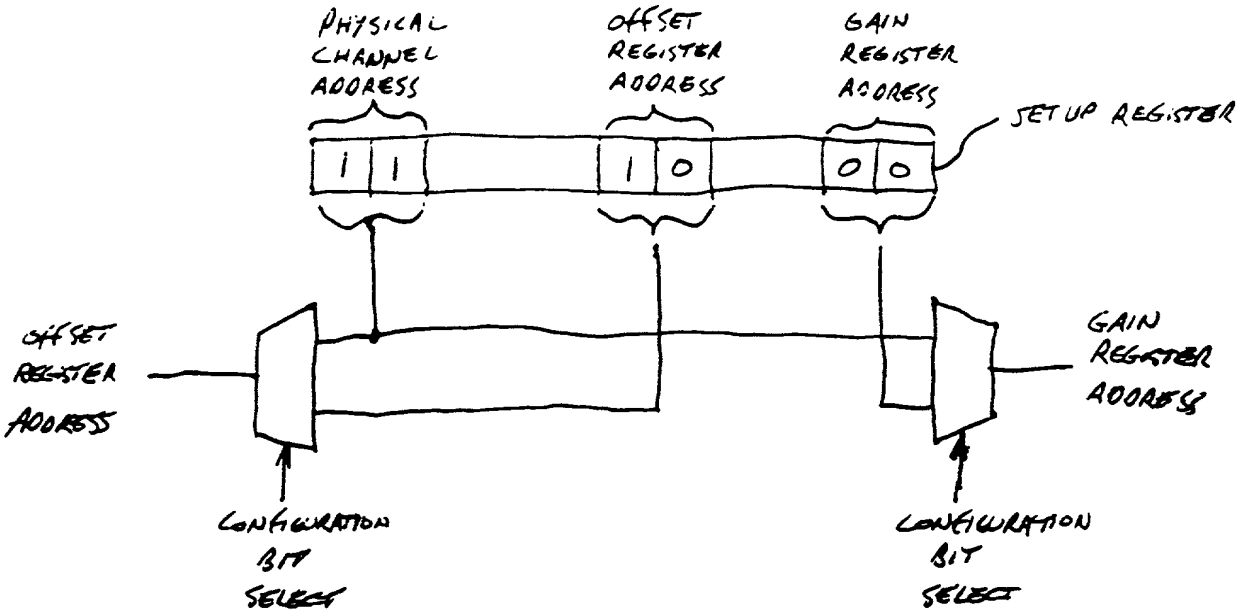

PHYSICAL CHANNEL ADDRESS
OFFSET REGISTER ADDRESS
GAIN REGISTER ADDRESS
SET UP REGISTER
1 1
1 0
0 0
OFFSET REGISTER ADDRESS
GAIN REGISTER ADDRESS
CONFIGURATION BIT SELECT
CONFIGURATION BIT SELECT

FIGURE 4.6

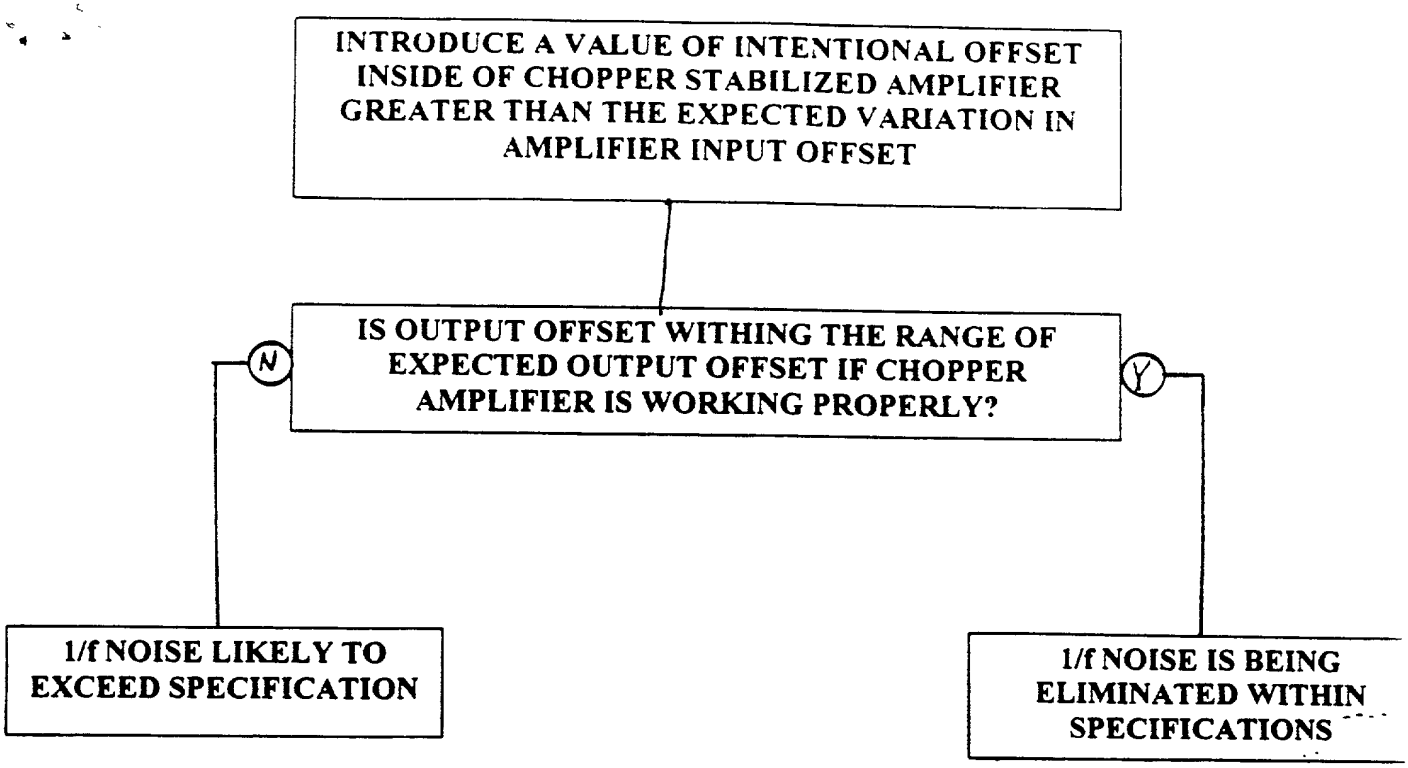

INTRODUCE A VALUE OF INTENTIONAL OFFSET INSIDE OF CHOPPER STABILIZED AMPLIFIER GREATER THAN THE EXPECTED VARIATION IN AMPLIFIER INPUT OFFSET
IS OUTPUT OFFSET WITHING THE RANGE OF EXPECTED OUTPUT OFFSET IF CHOPPER AMPLIFIER IS WORKING PROPERLY?
N
Y
1/f NOISE LIKELY TO EXCEED SPECIFICATION
1/f NOISE IS BEING ELIMINATED WITHIN SPECIFICATIONS

FIGURE 5.1

Thermocouple Application

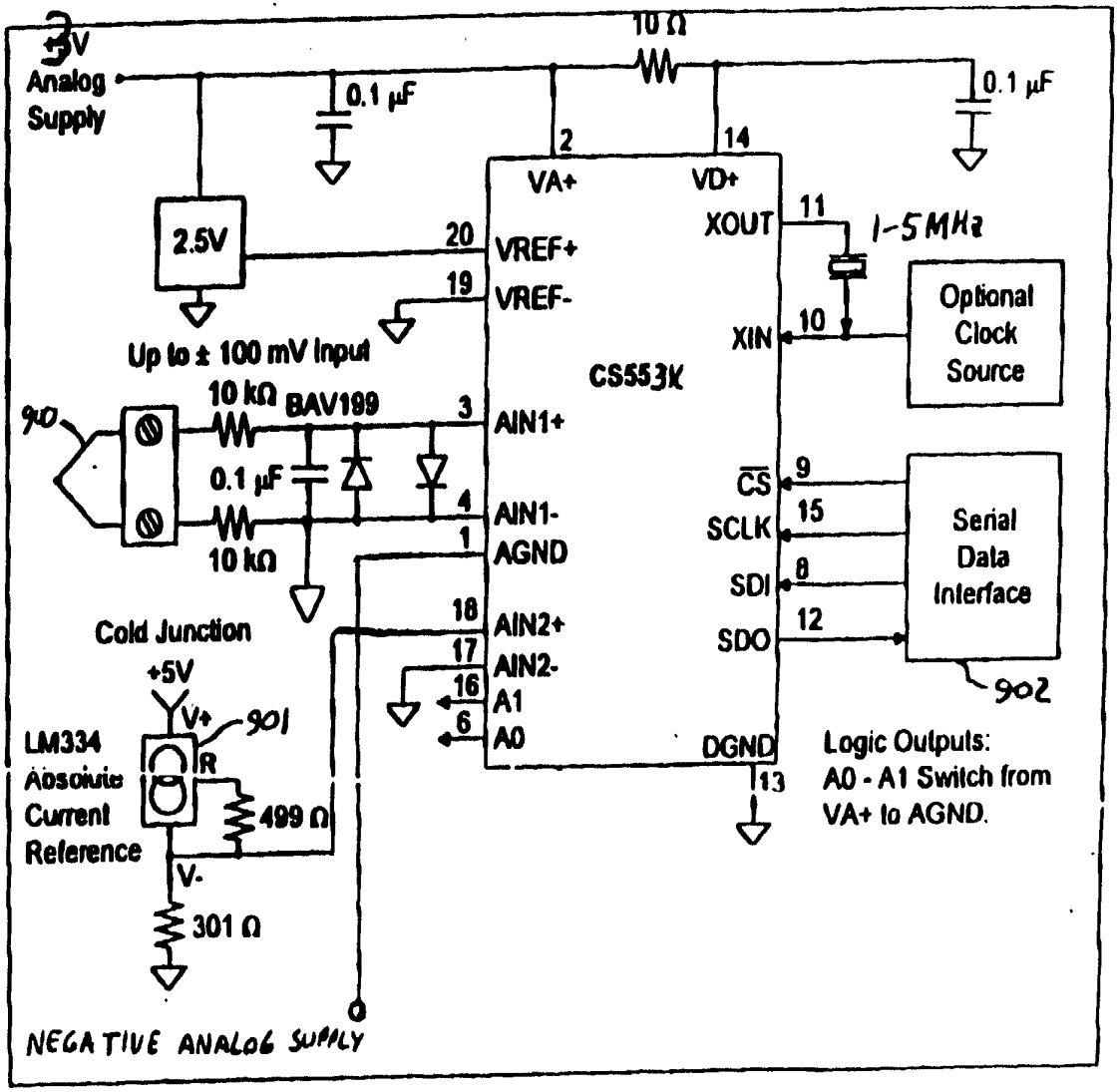


FIGURE 6.1

Bridge Transducer Application

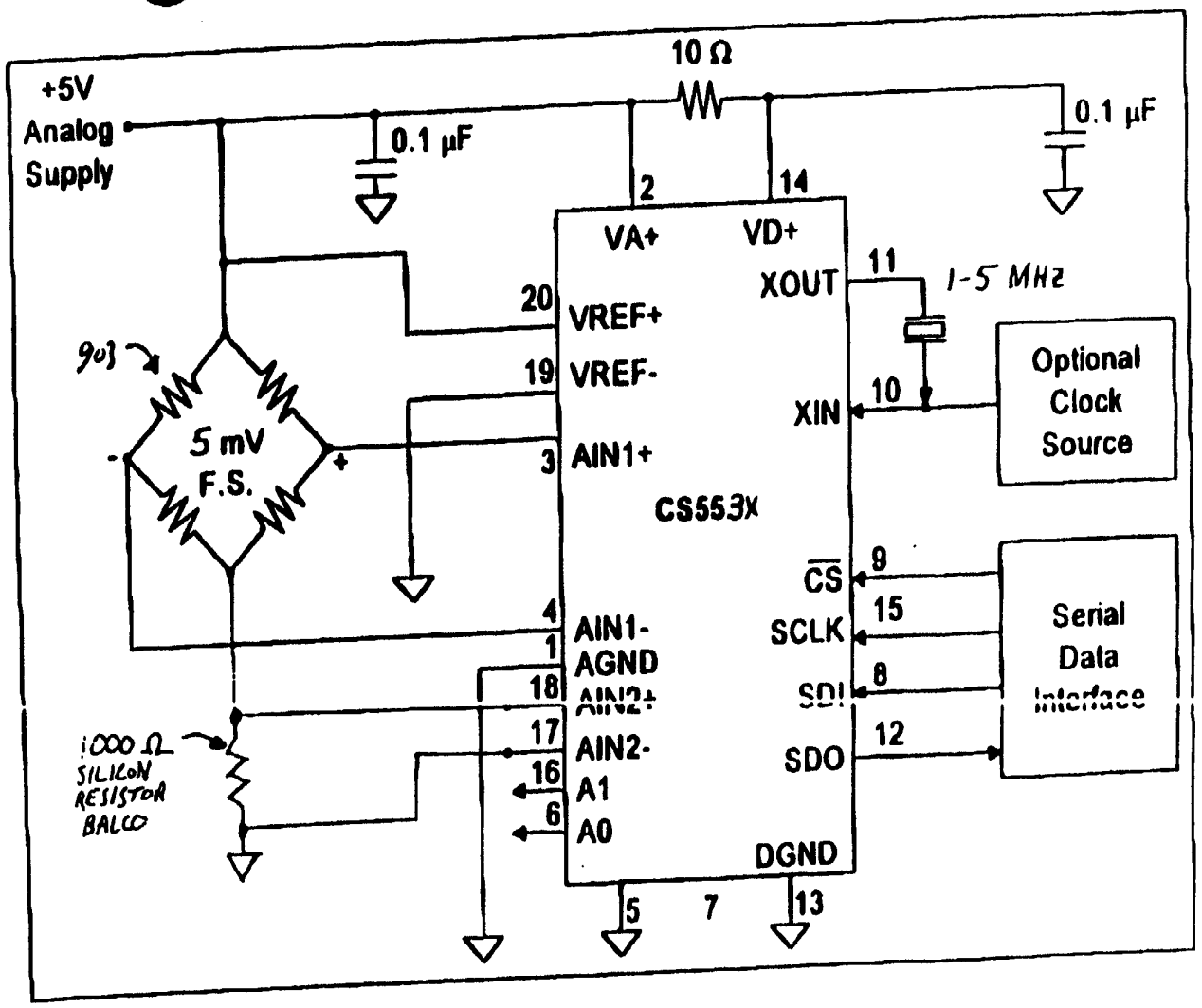


FIGURE 6.2